UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/985,693	11/05/2001	Thomas G. Ference	IBM: BUR919980202US2 - 21	4002

7590 06/24/2004

Connolly Bove Lodge & Hutz LLP
Suite 800
1990 M Street, N.W.
Washington, DC 20036-3425

EXAMINER	
GRAYBILL, DAVID E	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 06/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/985,693	FERENCE ET AL.	
	Examin r	Art Unit	
	David E Graybill	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *26-57* is/are pending in the application.

4a) Of the above claim(s) *33,34 and 46-49* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *26-32,35-45 and 50-57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11-5-1,6-7-2*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claims 33, 34 and 46-49 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 4-12-4.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 26, 28-30, 32, 35, 36, 45 and 50-57 are rejected under 35 U.S.C. 102(b) as being anticipated by Nishiguchi (5214308).

At column 4, line 41 to column 6, line 52, Nishiguchi discloses a method of fabricating a semiconductor structure, the method comprising: providing a first substrate 3 and a second substrate 1; providing contacts (5b and "spare solder") on one of the first substrate and the second substrate; providing first solder bumps 2a on one of the first substrate and the second substrate; mounting the first substrate on the second substrate; and reflowing the first solder bumps for surface tension aligning of the contacts; wherein at least one of the first substrate and the second substrate is an integrated circuit chip; wherein the contacts comprise second

solder bumps; further comprising: reflowing the second solder bumps, wherein the second solder bumps ball up to make contact between the first substrate and the second substrate; wherein the second solder bumps are provided with a smaller size than the first solder bumps; wherein reflowing the first solder bumps draws the first substrate toward the second substrate to cause the contacts to make contact with the first substrate and the second substrate; wherein the first solder bumps contact the first substrate and the second substrate prior to the contacts making contact between the first substrate and the second substrate; wherein the contacts are provided with a smaller size than the first solder bumps; wherein the contacts and the first solder bumps are provided such that an upper surface of the contacts and an upper surface of the first solder bumps are co-planar; wherein the contacts comprise at least one member selected from the group consisting of solder, a material other than solder, and PMC; further comprising: providing a ledge (narrow flat surface 5a) on at least one of the first substrate and the second substrate; wherein the first solder bumps are arranged in contact with the ledge, such that an upper surface of the contacts and an upper surface of the first solder bumps are co-planar; wherein the contacts are inherently (due to collapse of the first solder bumps) compressed as the first solder bumps are reflowed; further comprising arranging the first solder

bumps around a periphery of an area containing the contacts; wherein the step of reflowing the first solder bumps for surface tension aligning of the contacts includes aligning a plurality of controlled collapse chip connection contacts; further comprising ensuring that the first solder bumps are free of an electrical connection with any of the contacts; wherein the step of providing contacts on one of the first substrate and the second substrate comprises providing a plurality of second solder bumps each having a volume smaller than a volume of each of the plurality of first solder bumps.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 37 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishiguchi as applied to claim 26, and further in combination with Love (5773889).

Nishiguchi does not appear to explicitly disclose wherein the contacts are provided by thin film processing; wherein the thin film processing comprises lift off stencil or subtractive etch.

Notwithstanding, at column 3, lines 57-62, Love discloses wherein the contacts "solder" are provided by thin film processing; wherein the thin film processing comprises lift off stencil or subtractive etch.

Furthermore, it would have been obvious to combine this process of Love with the process of Nishiguchi because it would facilitate provision of the contacts of Nishiguchi.

Claims 39-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishiguchi (5214308).

Nishiguchi does not appear to explicitly disclose wherein the contacts each are provided with a diameter of less than about 50 μm; wherein the contacts each are provided with a diameter of about 10 μm; wherein the contacts each are provided with a diameter of less than about 10 μm;

wherein the contacts are provided with a pitch of less than about 100 μm; wherein the contacts are provided with a pitch of about 30 μm; wherein the contacts are provided with a diameter about 20% of the diameter of the first solder bumps.

Nevertheless, as cited supra, Nishiguchi discloses that both contact diameter and pitch are result-effective variables. Moreover, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed dimensional limitations because applicant has not disclosed that, in view of the applied prior art, the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using other dimensions. Indeed, it has been held that optimization of range limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See MPEP 2144.05(II): "Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. '[W]here the general conditions of a claim are disclosed in the prior art, it is not

inventive to discover the optimum or workable ranges by routine experimentation.'" In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). See also In re Hoeschele, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969), Merck & Co. Inc. v. Biocraft Laboratories Inc., 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989), and In re Kulling, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990). As set forth in MPEP 2144.05(III), "Applicant can rebut a prima facie case of obviousness based on overlapping ranges by showing the criticality of the claimed range. 'The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range.' In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990). See MPEP § 716.02 - § 716.02(g) for a discussion of criticality and unexpected results." Also, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338,

220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Claims 27, 31, 37, 39, 40, 41-44 and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishiguchi as applied to claims 26 and 29, and further in combination with Kashiba (JP06112463).

Nishiguchi does not appear to explicitly disclose the following wherein the contacts have a different composition than the first solder; wherein the second solder bumps comprise a material having a higher melting point that the first solder bumps, and reflowing the second solder bumps requires heating the second solder bumps to a higher temperature than reflowing the first solder bumps; wherein the contacts are provided by thin film processing; wherein the contacts each are provided with a diameter of less than about 50 μm; wherein the contacts are provided with a pitch of less than about 100 μm; wherein the contacts are compressed as the first solder bumps are reflowed.

Nonetheless, in the English translation, abstracts and figures, Kashiba discloses wherein the contacts 6a have a different composition than the first solder 5a; wherein the second solder bumps 6a comprise a material having a higher melting point that the first solder bumps, and reflowing the second solder bumps requires heating the second solder bumps to a higher

temperature than reflowing the first solder bumps; wherein the contacts are provided by thin film processing ("vacuum evaporation"); wherein the contacts each are provided with a diameter of less than about 50 μm; wherein the contacts are provided with a pitch of less than about 100 μm; wherein the contacts are compressed as the first solder bumps are reflowed.

Moreover, it would have been obvious to combine this process of Kashiba with the process of Nishiguchi because it would facilitate alignment.

However, neither Nishiguchi nor Kashiba appear to explicitly disclose wherein the contacts each are provided with a diameter of about 10 μm; wherein the contacts each are provided with a diameter of less than about 10 μm; wherein the contacts are provided with a pitch of about 30 μm; wherein the contacts are provided with a diameter about 20% of the diameter of the first solder bumps.

Regardless, as cited supra, both Nishiguchi and Kashiba disclose that contact pitch and diameter are result-effective variables. Moreover, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed dimensional limitations because applicant has not disclosed that, in view of the applied prior art, the limitations are for a particular unobvious purpose, produce an unexpected

result, or are otherwise critical, and it appears prima facie that the process would possess utility using another limitation.

Claim 38 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nishiguchi and Kashiba as applied to claim 37, and further in combination with Love.

Nishiguchi and Kashiba does not appear to explicitly disclose wherein the thin film processing comprises lift off stencil or subtractive etch.

Still, as cited supra, the combination of Nishiguchi and Kashiba discloses wherein the thin film processing comprises evaporation. In addition, as cited supra, Love disclose that evaporation and lift off stencil are equivalents; therefore, it would have been obvious to substitute or combine the lift off stencil of Love for or with the evaporation of Nishiguchi and Kashiba.

Claims 26-32, 35-37, 39, 42, 45 and 50-57 are rejected under 35 U.S.C. 102(b) as being anticipated by Kashiba (JP06112463).

As cited supra, Kashiba discloses a method of fabricating a semiconductor structure, the method comprising: providing a first substrate 1 and a second substrate 2; providing contacts 6a on one of the first substrate and the second substrate; providing first solder bumps 5a on one of the first substrate and the second substrate; mounting the first substrate

on the second substrate; and reflowing the first solder bumps for surface tension aligning of the contacts; wherein the contacts have a different composition than the first solder; wherein at least one of the first substrate and the second substrate is an integrated circuit chip; wherein the contacts comprise second solder bumps; further comprising: reflowing the second solder bumps, wherein the second solder bumps ball up to make contact between the first substrate and the second substrate; wherein the second solder bumps comprise a material having a higher melting point that the first solder bumps, and reflowing the second solder bumps requires heating the second solder bumps to a higher temperature than reflowing the first solder bumps; wherein the second solder bumps are provided with a smaller size than the first solder bumps; wherein reflowing the first solder bumps draws the first substrate toward the second substrate to cause the contacts to make contact with the first substrate and the second substrate; wherein the first solder bumps contact the first substrate and the second substrate prior to the contacts making contact between the first substrate and the second substrate; wherein the contacts are provided by thin film processing; wherein the contacts each are provided with a diameter of less than about 50 μm; wherein the contacts are provided with a pitch of less than about 100 μm; wherein the contacts are provided with a smaller size than the first

solder bumps; wherein the contacts and the first solder bumps are provided such that an upper surface of the contacts and an upper surface of the first solder bumps are co-planar; wherein the contacts comprise at least one member selected from the group consisting of solder, a material other than solder, and PMC; further comprising: providing a ledge (narrow flat surface) on at least one of the first substrate and the second substrate, wherein the first solder bumps are arranged in contact with the ledge, such that an upper surface of the contacts and an upper surface of the first solder bumps are co-planar; wherein the contacts are compressed as the first solder bumps are reflowed; further comprising arranging the first solder bumps around a periphery of an area containing the contacts; wherein the step of reflowing the first solder bumps for surface tension aligning of the contacts includes aligning a plurality of controlled collapse chip connection contacts; further comprising ensuring that the first solder bumps are free of an electrical connection with any of the contacts; wherein the step of providing contacts on one of the first substrate and the second substrate comprises providing a plurality of second solder bumps each having a volume smaller than a volume of each of the plurality of first solder bumps.

Claim 38 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kashiba as applied to claim 37 supra, and further in combination with Love.

Kashiba does not appear to explicitly disclose wherein the thin film processing comprises lift off stencil or subtractive etch.

Nonetheless, as cited supra, Kashiba discloses wherein the thin film processing comprises evaporation. In addition, as cited supra, Love disclose that evaporation and lift off stencil are equivalents; therefore, it would have been obvious to substitute or combine the lift off stencil of Love for or with the evaporation of Kashiba.

Claims 40, 41, 43 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kashiba (JP06112463).

Kashiba is applied for the same reasons it was applied to claims 26 and 37.

However, Kashiba does not appear to explicitly disclose wherein the contacts each are provided with a diameter of about 10 μm; wherein the contacts each are provided with a diameter of less than about 10 μm; wherein the contacts are provided with a pitch of about 30 μm; wherein the contacts are provided with a diameter about 20% of the diameter of the first solder bumps.

Regardless, as cited supra, Kashiba discloses that contact pitch and diameter are result-effective variables. Moreover, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed dimensional limitations because applicant has not disclosed that, in view of the applied prior art, the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another limitation.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any telephone inquiry of a general nature or relating to the status (MPEP 203.08) of this application or proceeding should be directed to Group 2800 Head SAE Linda Hodge-Taylor whose telephone number is 571-272-1585.

Any telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (571) 272-1930. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.

The fax phone number for group 2800 is (703) 872-9306.

David E. Graybill
Primary Examiner

Art Unit 2827

D.G.
22-Jun-04